

# Dicing Advanced Materials for Microelectronics

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**Abstract-** In recent years, the volume of thinned silicon and bumped silicon wafers have increased dramatically. The push to thinner silicon is driven by smart cards and stacked dice for low profile products which are highly popular in the marketplace. The dicing of advanced materials including thin wafers, ultra-thin silicon wafers, wafer with low k dielectric, bonded wafers and cavitated wafers is critically important for high volume IC production. Today, mechanical dicing with diamond saw blades remains the most cost effective manufacturing process. Advances in dicing processes and blade design allow for dicing of these wafers with minimum mechanical damage to the dice. Achieving end cut with no damage requires a fine balance between the design of the saw street dimension, the contents in the street and the wafer level processing that introduces internal stresses into the wafer. With the push to maximize die count per wafer, the saw street is often filled with wafer test features that not only degrade the cutting action of the blade but introduce internal stress in the silicon wafer. Data shows that chipping on redistributed and bumped wafers is higher than non-bumped wafers. This paper shows results from improved dicing parameters that will overcome yield loss during mechanical dicing without having to resort to laser dicing.

## I. INTRODUCTION

Die singulation is a major process that every single integrated circuit chip goes through. This is an intimate “meeting” of diamond and silicon from which every single chip is born. There is limited published attention and visibility on this process. With the trend towards wafer level packaging (WLP), thinner and low-K wafers, this singulation process becomes critical. Yield loss from stress damage by the dicing saw results in cracks into the active area of the die rendering it useless. Or cracks can initiate during the saw process and propagate into active area during reliability testing such as temperature cycling. Such cracks can be screened out but this additional process increases cost. Therefore, much effort is put into achieving no-damage (chipless) dicing. Achieving maximum yield during dicing is a concerted effort from the very beginning of the wafer and process design.

The industry is turning to laser dicing to offset some of the yield loss caused by mechanical dicing. The “meeting” of light and silicon is a new trend which may replace a lot of fragile wafers with low k components. However the need for mechanical dicing will not diminish as it works very well for thin silicon wafers, WLP wafers including bumped and redistributed wafers. These wafers have been successfully diced and the results are presented in this paper.

There are dozens of variables that go into mechanical wafer dicing[1]. One can do endless design of experiments of the dozens of variables affecting dicing to achieve less chipping and get confusing conclusions. However, the major variables

affecting chipping can be isolated from the rest and are listed here.

- Internal stress of wafer
- Blade selection
- Wafer mounting tape
- Speed of cut

## II. EXPERIMENT

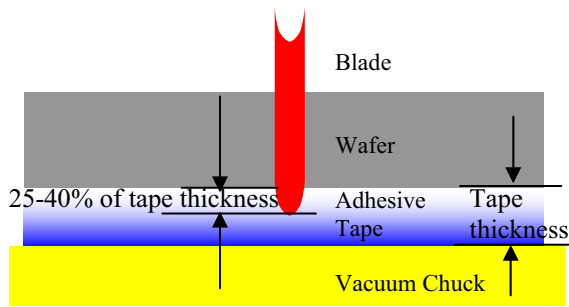
### A. Preparation of thinned wafer for Dicing

Blank silicon wafers were background at CORWIL Precision Wafer Thinning to 110  $\mu\text{m}$  in thickness with a 2000 grit finish. The intra to inter wafer thickness variation of all the blank wafers was 3  $\mu\text{m}$  total thickness variation. Five types of UV release wafer mounting tapes were procured from various suppliers including Nitto, Furukawa (2 types) and Lintec (2 types). Each tape has a peel strength which is in the medium to high tack range. No low tack tape was used. Non-UV wafer mounting tapes were not used because of poor release after dicing. The tape thicknesses range from 80  $\mu\text{m}$  to 130  $\mu\text{m}$ . All the wafers were mounted on each type of tape and manually centered inside a stainless steel film frame. The film frame allows the mounted wafer to be easily transported in cassettes without damage to the wafer.

The wafers were cut to a die size of 1.5 mm to 14 .0 mm with a length to width aspect ratio of greater than 9. A DISCO DAD 341 dicing saw from CORWIL was used. In this experiment, the machine set-up was optimized for chipless cutting using a commercially available blade. The following metal bonded hub blade was selected:

- Grit size: 2-4  $\mu\text{m}$  diamond
- Blade width: 15 to 20  $\mu\text{m}$
- Blade exposure: 300  $\mu\text{m}$

The dicing blade height was set so that the blade cuts 25 to 40% into the adhesive side of the tape thickness. Cutting this depth into the tape will eliminate a lip on the bottom corner edge of the die left by the bevel of the blade tip. Cutting >50% into the tape thickness will weaken the tape causing tearing in the subsequent pick and place process. The Disco DAD341 can control blade height to a precision of <0.1  $\mu\text{m}$ . See Figure 1 for an illustration of the blade-meets-silicon cross-section.



### B. Preparation of Bumped Wafer for Dicing

Additionally, a 200 mm bumped wafer with high proximity of bumps to a narrow saw street was diced as part of this study. See Figure 2 showing street proximity to peripheral bumps of the die. Eutectic lead-tin solder bumped wafers with polymeric coatings have built-up stress localized in the silicon under the bumps and can crack catastrophically during dicing. The bumped wafer was background to 300  $\mu\text{m}$  and sawn into 2 halves. One half was single cut while the other half was step (double) cut on Disco DFD 651 at CORWIL Technology. The DFD 651 is a dual spindle saw shown in Figure 3. The leading blade cuts a groove partially into the silicon street while the trailing blade cuts through the entire thickness of the wafer. Step or double cut has been successfully established to reduce chipping size in other applications. [2]



Figure 2. Bumps alongside of dicing street.

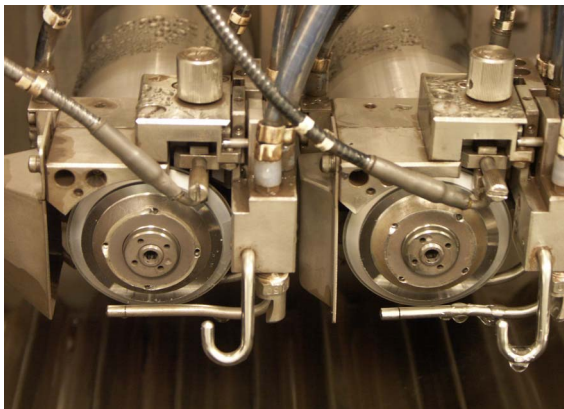


Figure 3. Dual spindle for step cutting.

### C. Post-dicing Procedure

After completing the dicing of the different groups of wafers, the taped wafers were exposed to ultraviolet (UV) light with a wavelength of 254 nm for 60 seconds using the ULTRON UV exposure machine. This UV exposure allows easy separation of the tape to the wafer. The calculated  $\text{mJ}/\text{cm}^2$  of this process is  $>500\text{mJ}/\text{cm}^2$  as recommended by all of the tape manufacturers. The wafers were then stretched on double hoop rings which widened the diced streets. This allowed each die to be ejected or removed from the tape without any contact to the adjacent die which may cause chipping.

The ejected dice were evaluated for sidewall chipping. The dice were mounted sideways with the diced wall facing up and put under an optical microscope so the chipping size can be measured. A sample size of 30 to 40 dice per group was used. If more than one crack exists on the sidewall of a single die, the worst case crack was measured. The chipping size was measured as a percentage of the die thickness. Military Standard 883 [3] for Class S and Class B applications requires that a die must be rejected if the chipping size is greater than 50% of the die thickness. This applies to cracks originating from the backside of the die extending into the top half of the die.

## III. RESULTS

### A. Results of the Thinned Silicon Wafer

The results show that various tapes do affect the sidewall chipping size and at least one tape (Tape B) stood out with no chipping on the sidewall of the thin silicon dice. It should be mentioned that the dicing saw parameters were optimized for minimum chipping and the critical variable in this experiment is the tape brands and their respective peel strengths. See Figure 4A. The high quality of the sidewall of the thinned silicon from Tape B is revealed in the photograph shown in Figure 4B.

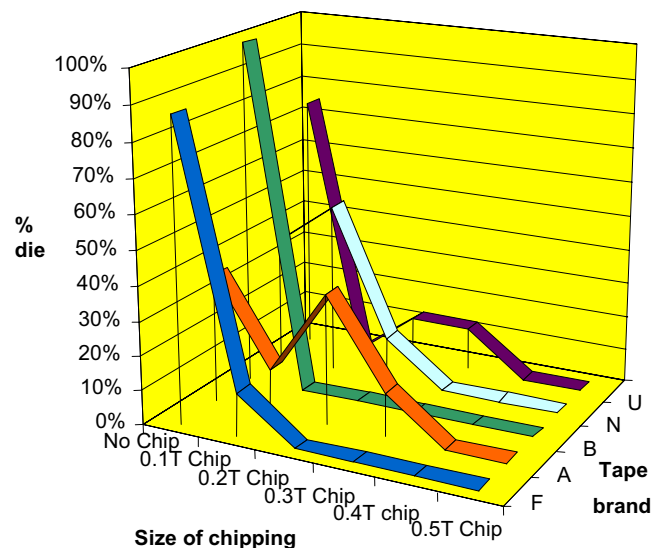


Figure 4A- Sidewall chipping size as % of die thickness.

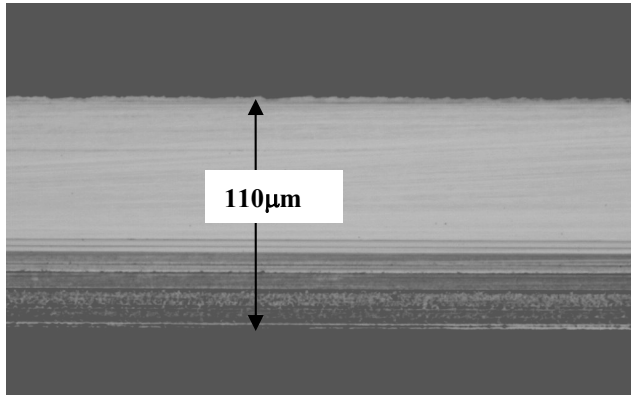


Figure 4B. Sidewall quality of die from Tape B.

On the backside of these diced wafers, the difference between the tapes is quite pronounced. Tape B with no sidewall chipping shows no backside chipping as well. However, Tape N with 30% of the dice showing 0.3 die thickness size sidewall chipping shows backside chipping as well. Figure 5A shows “J hook” shaped backside chipping indicating the direction of saw was from right to left. At the chipping size of approximately 50 µm, it is usually not a cause for alarm. For Tape B, no or negligible backside chipping was found as shown on Figure 5B. The photographs reveal the backside grind marks from the 2000 grit fine grind process. It is shown here that highly polished or chemically etched backside is not critical to achieving chipless dicing using conventional dicing method.

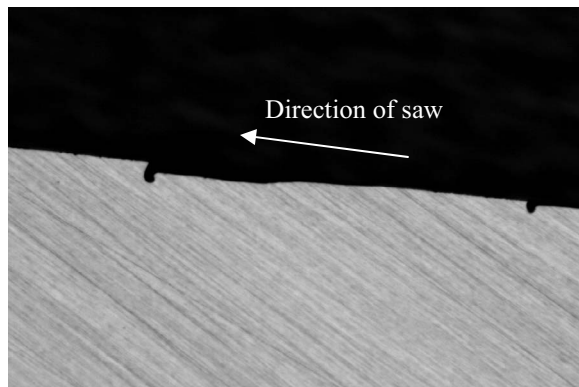


Figure 5A. Backside chipping of Tape N.

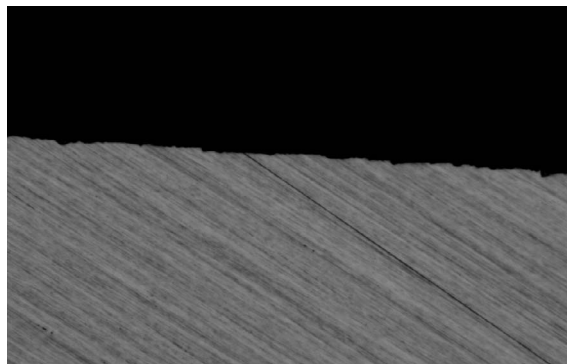


Figure 5B. Backside chipping (or lack off) of Tape B.

The same type of dicing blade was used in all 5 groups in this chipping comparison study. This blade is only 15 to 20 µm thin and is critical to chipless dicing. The final KERF width cut on this wafer is 20 µm only. This fineness of cut is almost comparable to laser dicing which can provide a KERF width of 10 µm. With such a fine cut, street dimensions for thinned silicon wafers can be reduced to as low as 40 to 50 µm, as long as there are no abnormal levels of stress from bumps or WLP processes.

#### B. Results of the Bumped Wafer

The results show a dramatic reduction in the sidewall chipping and cracking by switching to the step (double) cut mode of dicing. 90% of the dice do not have chipping and the rest with chipping lower than 10% of the die thickness or 30 µm in size or less. See graphed results shown in Figure 6. The grooving effect of the leading blade drastically reduces the backside chipping by relieving the stress from the silicon bulk and concentrating the stress right at the street lane.

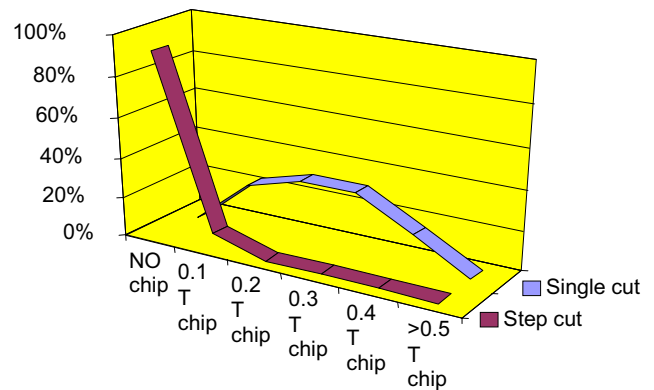


Figure 6. Comparison of single vs. step cut of a bumped wafer.

With step cut, chipping in bumped wafers shown in Figure 7A can be eliminated and flipchip dies free of sidewall chipping can be achieved. See Figure 7B.

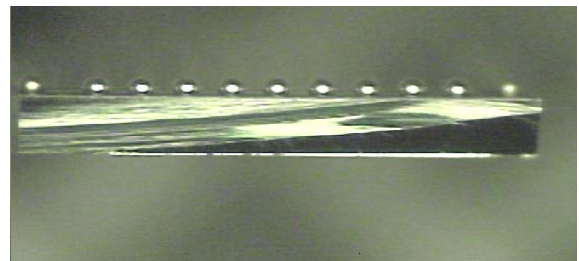


Figure 7A. Single cut bumped die with rejectable crack (>50% die thickness) on the sidewall.

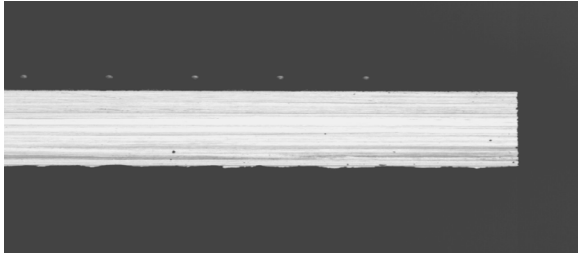


Figure 7B. Step cut bumped die with no sidewall crack.

#### IV. CONCLUSION

With the push towards wafer level packaging and ultra thin wafers for smart card and stacked die applications, singulating die with no chipping is achievable with mechanical dicing methods. It is imperative that dicing parameters be adjusted to relieve the stresses in the wafer. Using step cutting, the initial grooving of the first cut relieves the stress in the wafer allowing the rest of the wafer to be singulated without rejectable cracking. Variables like the proper selection of blades, proper selection of wafer mounting tape and machine set-up must be catered to such wafers with high stress. Additionally, wafers background with 2000 grit without final polish or chemical etching can yield chipless dice for silicon wafers which are 110  $\mu\text{m}$ . Data from other work which is not discussed in this paper indicates that chipless dice can be achieved for wafer thickness as low as 75  $\mu\text{m}$ . It has been shown that with the proper selection of machine parameters, blade type and wafer mounting tapes, chipless dice can be produced without having to switch to higher cost laser dicing.

#### ACKNOWLEDGMENT

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- [3] Military Standard 883, Method 2010, "Internal Visual".