A Memory Supplier's Outlook On Die Products

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Abstract

Mobile PCs and servers, wireless handsets, personal appliances and other mobile applications are driving the need for high-performance, low-cost, small form factor memory solutions. For this reason, die products as well as integrated packaging technologies are increasingly more prevalent as memory solutions designed into these applications. System designs are increasingly implementing integrated packaging strategies, such as the multichip package (MCP) or stacked package and system in package (SiP) products. The growth in die product demand is reflected in semiconductor manufacturers development of new production and test processes to enable the production of die products with a higher yield. The applications integrating die products are diverse, each one with its own form factor and device characteristic requirements. The emergence of several new packaging and die product solutions offers designers options and the ability to pick the technology that best meets their design requirements.

The wafer level chip scale package (WLCSP) is an example of an emerging packaging technology. WLCSP with a redistribution layer (RDL) applied provides many advantages over the standard thin small outline package (TSOP) and ball grid array (BGA) packages including electrical, thermal, and mechanical properties.

Market Requirements Driving Die Market

The markets driving the need for die products are also diverse, covering a plethora of applications. The catalyst within the mobile PC and server products market applications is their small form factor requirement as well as their need for increasing memory density on the memory modules. Both of these markets require higher memory densities in increasingly smaller form factors. The mobile PC application requirement is for the small-outline dual in-line memory module (SODIMM). As the overall system form factor shrinks, the outline of the DIMM reduces. The initial form factor of the SODIMM for SDRAM architectures is 67.6mm x 1.25in. and the smallest DDR SDRAM requirements is 67.6 mm x 1.0 in.

The form factor for the SDRAM registered DIMM popular in server applications is 5.25 in. x 1.7 in. and a reduced form factor for the DDR SDRAM registered DIMM is 5.25 in. x 1.2 in. Increases in memory density result in increased die size. On a one gigabyte (GB) registered DIMM there are thirty-six 512-megabit (Mb) devices. The standard approach to configuring numerous components on a registered DIMM form factor is to stack the packaged TSOPs with nine stacks per side. Another approach places all the memory devices in a planar configuration. The package outline reduction achieved with a WLCSP over the TSOP enables placement of the individual memory devices on the DIMM, eliminating the need for stacking.

Also driving the need for die products are the wireless mobile phone and handset applications. Wireless/mobile applications are also focused on small form factors and increased performance through higher density memory devices. Development of new integrated packaging technologies addressing the changing memory requirements resulting from the proliferation of new features and functionality emerging in wireless/mobile applications is a focus throughout the semiconductor industry. Currently, mobile applications are implementing a couple of approaches, MCP or stacked and SiP. Stacking memory devices in the same package is commonly referred to as a MCP. Integration, combining the ASIC and memory into one package, is commonly known as SiP.

Process of Packaging and Testing Die Products

Process flows for packaging and testing die products depend on the application form factor and the level of quality needed. If the die are sold in wafer form and packaged by the end customer a probe-based test process, also referred to as a known good die (KGD) flow, occurs prior to shipping the wafer. Achieving a low-cost, high-quality KGD process is an increasing need and in most high-volume DRAM test flows in not a reality today. A probe test flow yielding a memory device with a high quality level equal to a standard SDRAM is not a cost effective solution for many of today's applications. In addition to the cost challenge there is an engineering challenge to develop a reliable contact technology, testing many devices in parallel while exposing the wafers to temperature excursions. The best way to reduce costs in a probe test flow is to eliminate as many tests as possible after fully characterizing the design and process characteristics of the memory device. A possible KGD flow would be WLBI or a heat/voltage stress - Function Test - Speed Test.

The high-density module application offers a different package and test flow. In this application, the bond pads are redistributed over the surface of the die to ball pads arranged in an array. This is commonly referred to as a redistribution layer (RDL). Conductive balls are then attached to the ball pads on the wafers. The ball or bump attach process is performed with either a screen print process or placement of preformed solder balls. In a standard memory package process the individual silicon die are assembled on to metal lead frames and encapsulated. This basic assembly or packaging process provides the electrical connection to the

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devices and gives it a protective shell. The form factor of a WLCSP requires application of the electrical connection and protective shell within the physical die size constraints. In this application the RDL provides the electrical interconnection. To keep the silicon from being damaged during the test and module assembly process the application of a protective layer to the die is necessary. A thick polymer layer can be applied as the protective layer in place of the standard mold compound.

As a product architecture and density transitions from one fab process node to another, the size of the die changes. This creates added infrastructure cost to back-end test equipment, requiring new sockets and load boards to facilitate the new die size. If the ball grid is not designed considering the process migration and die size change, design of a new ball grid with a smaller pitch is necessary. Designing the ball grid small enough for use through two process nodes is recommended to offset additional costs incurred from changes. If the grid remains the same, the socket and infrastructure can be designed with an insert that can be exchanged to facilitate the new die size.

Electrical, Mechanical and Thermal Properties

As the density and operating frequencies increase for the high-density module application there are significant electrical, thermal, and mechanical advantages to a WLCSP with an RDL applied. WLCSP possesses several thermal advantages to other chip scale package (CSP) or BGA package technologies. Improved thermal integrity and dissipation are significant considerations for many new designs. The DDR SDRAM and SDRAM memory devices dissipate up to .5W per device. This power consumption generates high temperature conditions on die, degrading the device's performance. The TSOP and FBGA packages contain materials, such as mold compound or a substrate, between the surface of the die and the ambient air. These materials create a thermal barrier and act as an added thermal resistance to the device's heat dissipation. Today's emerging memory architectures include clock and data frequency targets, increasing the power consumption of the memory devices. The increasingly smaller system form factors emerging in the market provide minimal air space for increased airflow. The confined space and low airflow contributes to higher system ambient temperatures. The cross sections of the packages below show the additional materials contained in TSOP and FBGA packages. Since the silicon makes up a majority of the WLCSP package, as shown in the cross section below, there is no barrier between the ambient air and the device.

Signal Integrity, or electrical performance, is very important for the new high-speed memory architectures. For most applications the electrical characteristics of the package are: inductance (L), capacitance (C), and resistance (R) of interconnects. The L, C, and R of the package are dependent upon frequency, power and the ground reference proximity to conductors, and material properties. The TSOP and BGA architectures provide relatively higher inductance and thus higher signal degradation, reducing the ability for power and ground connections to supply the instantaneous current demands of the die. The WLCSP offers lower inductance values resulting from the elimination of wire bonds and internal leads associated with conventional TSOP or FBGA designs. The path from the traditional wire bond pad to the ball pad is replaced by a short, direct electrical connection resulting in a significant increase in electrical performance. The inductance of the TSOP and BGA packages is becoming more problematic in the power supply interconnects for the new memory architectures. The BGA package has been defined as the standard for DDR2 SDRAM. As the industry pushes higher in clock and I/O performance, minimizing the inductance is required to maintain signal integrity.

The solder joint reliability of the memory device interconnects on the high density modules are improved with the addition of under-fill between the device and the printed circuit board (PCB). Temperature cycle testing reflects a significant improvement in performance of the WLCSP with under-fill over a TSOP package. The under-fill material acts as a glue to lock the package and PCB together, ensuring the solder ball to pad interface is not over stressed.

Conclusions

In conclusion there is a great amount of interest in die products from the established and emerging markets. To meet these market needs the memory suppliers need to continue development of wafer level chip scale package architectures and probe based test flows. The memory supplier with the highest quality die products and lowest cost well positioned to gain market share.

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